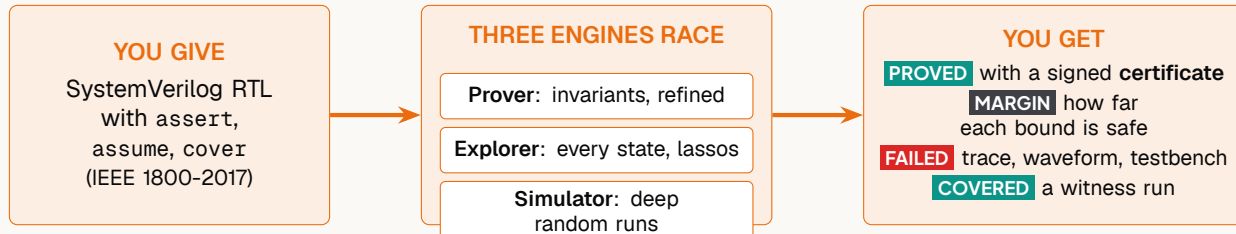


SystemVerilog Assertion Verifier

Prove every assertion of your RTL design, for all inputs and every start state, get a certificate your customer can check, and know how much safety margin each proof has.

Formal verification of SVA · no test vectors · runs on your computer, offline



One command

```

$ sva-verify --reset=rst --report=cert buffer.sv
PROVED    assert    margins.a_level
PROVED    assert    margins.a_latency
Safety margins:
a_level   level <= 12 margin 3
a_latency ##[1:6]   margin 3 cycles
Giolit Safety Resilience Score: ★★★★★★
Report: cert/certificate.pdf
  
```

Exit codes and JSON for CI; a C++ SDK for your own tools.

What it handles

- ✓ SVA sequences and properties: `##[m:n]`, `[*]`, `[->]`, `|->`, `|=>`, `until`, ...
- ✓ **Liveness**: `s_eventually`, `k-liveness` proofs, lasso counterexamples
- ✓ Assumptions, covers, immediate assertions, `$past`, `$stable`
- ✓ Hierarchy, parameters, generate, interfaces, packages, bind
- ✓ One global clock or exact multi-clock semantics
- ✓ Every engine built in-house: no external solver

Only in Giolit

🔧 Proof certificates

Every PROVED comes with its proof: the **inductive invariant** of the design, in your own signal names, that holds at the first clock edge, survives every clock cycle and excludes the failure – checkable by hand. The PDF certificate, waveforms and replay testbenches are bound by SHA-256 in a statement **signed** with your key; your customer runs one script to check it.

Inv: `b = a ^ 0 <= b <= 12000000`

🔍 Safety margins

A proof says an assertion holds; the margin says **by how much**. For every proved bound (`count <= DEPTH`) and latency window (`##[1:6]`) the verifier proves tightened versions until one fails: the distance between what the design does and what it may never do. The weakest bound gives the **Giolit Safety Resilience Score**, ★☆☆☆☆ to ★★★★★.

Zero margin: any change toward the bound turns the verdict.

Measured against SymbiYosys and EBMC

	Giolit	SymbiYosys	EBMC 6.0
EBMC regression suite: correct, of 168	163	55	114
SymbiYosys examples: correct, of 63	56	49	46
TACAS 2016 designs decided, of 12	4	7	6
Wrong answers, on 340 properties	0	–	–
Proof certificate (signed invariant)	✓	–	–
Safety margin and resilience score	✓	–	–

Designs decided correctly, same 20 s budget per design for every tool; SymbiYosys with `abc pdr`, EBMC with a portfolio of its engines (k-induction, IC3, BDD, bounded). EBMC and SymbiYosys decide more of the bit-level TACAS 2016 designs. Every result: the Tool Comparison and the package's results/ folder.

All 231 designs with a known answer



Try it: free trial, 1000 runs in 50 days

Linux x86-64 (Ubuntu 24.04) · professional licenses by term and volume

verification services: properties written and proved by Giolit engineers

 www.giolit.com

✉ business.giolitlabs@gmail.com

Giolit Labs, Thrissur, Kerala, India